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23529 7590 07/01/2008

ADE & COMPANY INC.
2157 Henderson Highway
WINNIPEG, MB R2G1P9
CANADA

EXAMINER

TORRES, JUAN A

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 07/01/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/796,416

03/10/2004

Gerald Harron

85195-502 ADB

9044

TITLE OF INVENTION: METHOD AND APPARATUS FOR DIGITAL VECTOR QAM MODULATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	10/01/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23529 7590 07/01/2008

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CANADA

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/796,416 03/10/2004 Gerald Harron 85195-502 ADB 9044

TITLE OF INVENTION: METHOD AND APPARATUS FOR DIGITAL VECTOR QAM MODULATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional YES \$720 \$300 \$0 \$1020 10/01/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
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TORRES, JUAN A 2611 375-298000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Date _____

Typed or printed name _____

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,416	03/10/2004	Gerald Harron	85195-502 ADB	9044
23529	7590	07/01/2008	EXAMINER	
ADE & COMPANY INC. 2157 Henderson Highway WINNIPEG, MB R2G1P9 CANADA			TORRES, JUAN A	
			ART UNIT	PAPER NUMBER
			2611	
DATE MAILED: 07/01/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 935 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 935 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/796,416

Examiner

JUAN A. TORRES

Applicant(s)

HARRON ET AL.

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment - After Non-Final Rejection filed on 02/28/2008.
2. ☒ The allowed claim(s) is/are 1-33.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other ____. |

DETAILED ACTION

Drawings

The modifications to the drawings were received on 02/28/2008. These modifications are accepted by the Examiner.

In view of the amendment filed on 02/28/2008, the Examiner withdraws Drawing objections of the previous Office action.

Specification

The modifications to the specification were received on 02/28/2008. These modifications are accepted by the Examiner.

In view of the amendment filed on 02/28/2008, the Examiner withdraws Specification objections of the previous Office action.

Claim Objections

The modifications to the claims were received on 02/28/2008. These modifications are accepted by the Examiner.

In view of the amendment filed on 02/28/2008, the Examiner withdraws claim objections to claim 4, 5, 14, 16, 20, 21 and 27 of the previous Office action.

Claim Rejections - 35 USC § 112

The modifications to the claims were received on 02/28/2008. These modifications are accepted by the Examiner.

In view of the amendment filed on 02/28/2008, the Examiner withdraws claim rejections under 35 USC § 112 second paragraph to claims 8, 26 and 31 of the previous Office action.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Adrian D. Battison on 6/25/2008.

The application has been amended as follows:

A completed text for all the claims follows:

"Claims:

1. An apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing an input signal having a series of reference pulses at a frequency of the high speed reference clock which is higher than a desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses from the high speed reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors; and

a signal combining element for receiving the fixed amplitude output digital vectors from the two digitally controlled programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated and in which the desired output frequency is determined by an increment value.

2. An apparatus for directly generating a QAM RF signal comprising:

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a high speed reference clock providing an input signal having a series of reference pulses at a frequency of the high speed reference clock which is higher than a desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses from the high speed reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors; and

a signal combining element for receiving the fixed amplitude output digital vectors from the two digitally controlled programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated; wherein there are provided amplifiers for amplifying the two fixed amplitude output digital vectors non linearly before combining.

3. The apparatus according to claim 1 wherein the two digitally controlled programmable digital delay elements comprise high speed adders/accumulators wherein said high speed adders/accumulators are arranged to determine an amount of delay implemented by the two digitally controlled delay elements on the high speed reference clock.

4. An apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing an input signal having a series of reference pulses at a frequency of the high speed reference clock which is higher than a desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses from the high speed reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors; and

a signal combining element for receiving the fixed amplitude output digital vectors from the two digitally controlled programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated;

wherein the two digitally controlled programmable digital delay elements comprise high speed adders/accumulators wherein said high speed adders/accumulators are arranged to determine an amount of delay implemented by the two digitally controlled delay elements on the high speed reference clock; and wherein an increment value is set according to the following equation:

$$\text{Increment Value} = ((f_{\text{ref}}/f_{\text{out}} - 1) * 2^n)$$

where f_{ref} = Reference clock frequency

f_{out} = Desired output frequency

n = Number of bits in accumulator math.

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5. An apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing an input signal having a series of reference pulses at a frequency of the high speed reference clock which is higher than a desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses from the high speed reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors; and

a signal combining element for receiving the fixed amplitude output digital vectors from the two digitally controlled programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated;

wherein the two digitally controlled programmable digital delay elements comprise high speed adders/accumulators wherein said high speed adders/accumulators are arranged to determine an amount of delay implemented by the two digitally controlled delay elements on the high speed reference clock signal; and

wherein a duty cycle of the two fixed amplitude output digital vectors is set by initializing a difference of initializing values of two accumulators according to the following equation: the high speed reference clock frequency divided by the desired output frequency multiplied by 2^n , multiplied by $(p/100)$, where p is a percentage duty cycle and n is a number of bits in the accumulator math.

6. The apparatus according to claim 1 wherein said high speed reference clock is an external input with high frequency absolute accuracy and very low phase noise performance.

7. The apparatus according to claim 1 wherein said two digitally controlled programmable delay elements delay a reference edge of the input high speed reference clock.

8. The apparatus according to claim 7 wherein said reference edge of the input high speed reference clock may be either a rising or falling edge of the high speed reference clock.

9. The apparatus according to claim 1 wherein said two digitally controlled delay elements have separate controls for producing a rising and falling edges of an output from a same input edge of the high speed reference clock.

10. The apparatus according to claim 1 wherein implementation of the two digitally controlled delay elements may vary by altering the input high speed reference clock signal.

11. The apparatus according to claim 3 wherein said adders/accumulators are arranged to determine the amount of digitally controlled delay implemented by the two digitally controlled delay elements on the high speed reference clock to produce the desired RF frequency.

12. The apparatus according to claim 1 wherein said two digitally controlled programmable digital delay elements include modulation adders which add in a positive or negative phase offset to an accumulator value to produce a required modulation.

13. The apparatus according to claim 1 wherein there is provided an interpolator which interpolates the input data in the form of base band modulated information.

14. The apparatus according to claim 13 wherein the interpolator is a linear interpolator or a $(\sin x)/x$ interpolator filter.

15. The apparatus according to claim 13 wherein the interpolator effects interpolation up to the high speed reference clock rate so as to avoid the use of a reconstruction filter.

16. The apparatus according to claim 1 wherein there are provided separate interpolators for both the rising and falling pulse edges.

17. The apparatus according to claim 1 wherein there is provided a pulse swallow circuit which is arranged to ignore/block multiple high speed reference clock pulses.

18. The apparatus according to claim 17 wherein the pulse swallow circuit is arranged such that it is controlled by carry bits (overflow bits) in order to extend the delay to multiple cycles of the input high speed reference clock.

19. The apparatus according to claim 17 wherein said pulse swallow circuit is located prior to or following each of the two digitally controlled programmable delay elements.

20. The apparatus according to claim 1 wherein the two digitally controlled programmable digital delay elements are arranged such that 360 degrees of phase delay of the digitally controlled programmable delay is calibrated to 2^n of a phase accumulator value using a look up table or microprocessor.

21. The apparatus according to claim 20 wherein the lookup table has a multiple set of lookup tables to be used for temperature compensation of the two digitally controlled programmable delay elements.

22. The apparatus according to claim 1 wherein said signal combining element comprises flip-flops which are used to combine the separate rising and falling edge delays to form any desired duty cycle output.

23. The apparatus according to claim 22 wherein the two digitally controlled programmable digital delay elements are arranged such that said duty cycle of the output is varied by changing the difference in the initialization values of accumulators for the rising and falling edge delay control.

24. The apparatus according to claim 22 wherein the two digitally controlled programmable digital delay elements are arranged such that said output duty cycle is not dependent on the input duty cycle.

25. The apparatus according to claim 22 wherein the phase modulated vector outputs of the flip-flops is amplified using nonlinear amplifiers.

26. The apparatus according to claim 8 wherein increment values for the rising and falling edges are the same value.

27. The apparatus according to claim 3 wherein the two digitally controlled programmable digital delay elements are arranged such that a worst case frequency resolution is determined by the equation: the high speed reference frequency divided by 2^n , where n is equal to the number of bits in an accumulator.

28. The apparatus according to claim 3 wherein the two digitally controlled programmable digital delay elements are arranged such that increasing the number of bits in the adder math increases the frequency resolution with negligible degradation in the phase noise performance.

29. The apparatus according to claim 3 wherein the two digitally controlled programmable digital delay elements are arranged such that the number of bits of math used in the adders/accumulators can be equal to or exceed the number of bits of control in lookup table and/or the programmable delay.

30. The apparatus according to claim 3 wherein the two digitally controlled programmable digital delay elements include parallel processing in the adders and/or accumulators to increase the speed.

31. The apparatus according to claim 3 wherein the two digitally controlled programmable digital delay elements are arranged such that the adders/accumulators are implemented in a lookup table containing data which is pre-computed and stored.

32. The apparatus according to claim 1 wherein the apparatus is formed fully digitally in an application-specific integrated circuit (ASIC) with no requirement for a voltage controlled oscillator, loop filter, or digital to analog converter. “

33. The apparatus according to claim 1 wherein there is further provided amplification and filtering of an output QAM RF signal to produce a signal that is higher in amplitude and/or having fewer harmonics.”

Allowable Subject Matter

Claims 1-33 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 1-33 are allowed because a comprehensive search of prior art failed to teach, either alone or in combination, a high speed reference clock providing in an input signal having a series of pulses at a frequency of the high speed reference clock which is higher than a desired output frequency, two digitally controlled programmable digital delay elements each arranged to receive reference pulses from the high speed reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors, and a signal combining element for receiving the fixed amplitude output digital vectors from the two digitally controlled programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated and in which the desired output frequency is determined by an increment value, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
6-25-2008

/Juan A Torres/
Examiner, Art Unit 2611